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REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. Claim amendments are presented herein to obviate the current rejection.

35 USC § 102 / 35 USC § 103

Claims 1, 4, 7-17, and 20-25 stand rejected under 35 USC § 102(b) as allegedly being clearly anticipated by Byrne. Claim 19 stands rejected under 35 USC § 103(a) as allegedly being unpatentable over Byrne in view of Tran. Claims 26-30 stand rejected under 35 USC § 103(a) as allegedly being unpatentable over Byrne. These rejections are respectfully traversed.

Claim 1 recites piping a second of said loop conditions from said first pipeline of the pipelined processor to a second pipeline of the pipelined processor. Claims 13 and 26 recite similar features. In addition, claims 7, 22, and 26 have been amended to recite similar features.

Instruction 502 of Byrne is cited as disclosing each and every limitation of claim 1. However, it is respectfully submitted that Byrne (whether with regard to instruction 502 or otherwise) fails to disclose, inter alia, piping loop conditions from one pipeline to another pipeline. Instruction 502 acts to decrement a base address value in register r6 by 8 bytes.

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Moreover, Byrne describes an arrangement in which pipelined floating point execution units simultaneously receive identical instruction signals (see, inter alia, Byrne col. 6, lines 20-24). Therefore, with Byrne, instructions are initially fed to each pipeline as opposed to being piped from one pipeline to another.

Accordingly, the claims should be allowable.

Concluding Comments

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed.

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